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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,300	12/04/2003	Peter T. Freiburger	ROC920030284US1	7114

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EXAMINER	
KIM, HONG CHONG	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,300	FREIBURGER ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-17 are presented for examination. This office action is in response to the application filed on 12/4/2003.

Information Disclosure Statement

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. " first and second word lines" and "first and second memory arrays" aspects of the invention should be mentioned in the title so that the title is more descriptive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumar et al. (Kumar) US Patent No. 6,016,534.

As to claims 1 and 8, Kumar discloses a method for writing a least recently used (LRU) indicator (Fig.3) comprising: activating one of a first word line (col. 3 lines 50-65, 130 deep reads on this limitation) that corresponds to a first memory array (Fig.3 Ref. 309) and a second word line (col. 3 lines 50-65, 130 deep reads on this limitation) which corresponds to a second memory array (Fig. 3 Ref. 305); employing the first word line, when activated, for writing to the first memory array (Fig. 3 Ref. 302 and col. 4 lines 13-26) and for writing the LRU indicator; and employing the second word line, when activated, for writing to the second memory array and for writing the LRU indicator (Fig. 3 Ref. 302 and col. 4 lines 13-26).

As to claims 2 and 9, Kumar further discloses setting a signal on a first and second bit line to a first logic state (col. 4 lines 13-25, powered up state read on this limitation since it will clear all LRU bits).

As to claims 3 and 10, Kumar further discloses wherein setting a signal on the first and second bit line to a first logic state includes setting a signal on the first and second bit line to a low logic state (col. 4 lines 12-25, definition of binary bit reads this limitation, since it can be either 0 or 1).

As to claims 4 and 11, Kumar further discloses activating one of the first word line that corresponds to the first memory array and the second word line which corresponds to the second memory array includes setting a signal on one of the first word line and the second word line to a second logic state (col. 4 lines 12-25, setting and resetting LRU bit reads this limitation).

As to claims 5 and 12, Kumar further discloses setting a signal on one of the first word line and the second word line to a second logic state includes setting a signal on one of the first word line and the second word line to a high logic state (col. 4 lines 12-25, setting and resetting LRU bit reads this limitation).

As to claims 6 and 13, Kumar further discloses employing the first word line, when activated, for writing to the first memory array and for writing the LRU indicator includes employing the first word line, when activated, for writing to the first memory array and for activating a first port of a cell (LRU bit for each array row reads on this limitation) that stores the LRU indicator; and wherein employing the second word line, when activated, for writing to the second memory array and for writing the LRU indicator includes employing the second word line, when activated, for writing to the second memory array and for activating a second port of the cell that stores the LRU indicator (col. 4 lines 12-25, setting and resetting LRU bit reads this limitation).

As to claims 7 and 14, Kumar further discloses employing the first word line, when activated, for writing to the first memory array and for writing the LRU indicator includes employing the first word line, when activated, for writing to the first memory array and for storing a bit of a first logic state in a cell that stores the LRU indicator; and wherein employing the second word line, when activated, for writing to the second memory array and for writing the LRU indicator includes employing the second word line, when activated, for writing to the second memory array and for storing a bit of a second logic state in the cell that stores the LRU indicator (col. 4 lines 12-25, setting and resetting LRU bit reads this limitation).

5. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Battaglia US Patent Pub. No. 2003/0227801.

As to claims 1 and 8, Battaglia discloses a method for writing a least recently used (LRU) indicator (Fig. 3b) comprising: activating one of a first word line (Fig. 3B WL1) that corresponds to a first memory array (Fig. 1 DB's) and a second word line (Fig. 3B WLn) which corresponds to a second memory array ; employing the first word line, when activated, for writing to the first memory array and for writing the LRU indicator (Fig. 3B WL1); and employing the second word line, when activated, for writing to the second memory array and for writing the LRU indicator (Fig. 3B WLn).

As to claims 2 and 9, Battaglia further discloses setting a signal on a first and second bit line to a first logic state (block 68 col. 6).

As to claims 3 and 10, Battaglia further discloses setting a signal on the first and second bit line to a first logic state includes setting a signal on the first and second bit line to a low logic state (block 68 col. 6).

As to claims 4 and 11, Battaglia further discloses activating one of the first word line that corresponds to the first memory array and the second word line which corresponds to the second memory array includes setting a signal on one of the first word line and the second word line to a second logic state (block 68 col. 6).

As to claims 5 and 12, Battaglia further discloses setting a signal on one of the first word line and the second word line to a second logic state includes setting a signal on one of the first word line and the second word line to a high logic state (block 68 col. 6).

As to claims 6 and 13, Battaglia further discloses employing the first word line, when activated, for writing to the first memory array and for writing the LRU indicator includes employing the first word line, when activated, for writing to the first memory array and for activating a first port (block 66 dual-port SRAM cells) of a cell (Fig. 3a)that stores the LRU indicator; and wherein employing the second word line, when activated,

for writing to the second memory array and for writing the LRU indicator includes employing the second word line, when activated, for writing to the second memory array and for activating a second port of the cell that stores the LRU indicator (block 68 col. 6).

As to claims 7 and 14, Battaglia further discloses employing the first word line, when activated, for writing to the first memory array and for writing the LRU indicator includes employing the first word line, when activated, for writing to the first memory array and for storing a bit of a first logic state in a cell that stores the LRU indicator; and wherein employing the second word line, when activated, for writing to the second memory array and for writing the LRU indicator includes employing the second word line, when activated, for writing to the second memory array and for storing a bit of a second logic state in the cell that stores the LRU indicator (block 68 col. 6).

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (Kumar) US Patent No. 6,016,534 or Battaglia US Patent Pub. No.

2003/0227801 in view of Dawson et al. (Dawson)US Patent No. 4,995, 001.

As to claims 15-17, Kumar and Battaglia disclose the invention as claimed above however, neither Kumar nor Battaglia specifically discloses pass gate circuit.

Dawson discloses pass gate circuit (Fig. 6) for the purpose of providing high impedance between input and output and higher speed access.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate pass gate circuit as shown in Dawson into the combined invention of Kumar and Battaglia for the advantages stated above.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
571-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
April 26, 2006